UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,120	07/31/2003	Gerard Chauvel	TI-35486 (1962-05420)	3950

23494 7590 03/08/2007

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/631,120	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 7-28 are pending.

2. The office acknowledges the following papers:

Specification, arguments, and claims filed on 9/26/2006.

Withdrawn objections

3. The specification objections have been withdrawn due to amendment.

Maintained Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 7-12 and 14-16 are rejected under 35 U.S.C. §102(e) as being anticipated by Park et al. (U.S. 6,832,305).

6. As per claim 7:

Park disclosed a method, comprising:

Fetching and decoding instructions in a first processor (Park: Figure 1 element 120, column 3 lines 26-37)(The coprocessor is the first processor and has fetch and

decode abilities.);

Detecting an unsupported instruction that is not executable by the first processor (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects instructions that are executable by the CPU and not executable by the coprocessor. Thus having the same functionality.);

Executing said unsupported instruction in a second processor (Park: Figure 1 element 110, column 3 lines 26-37); and

Providing the first processor with a supported instruction that is executable in the first processor without the first processor fetching said instruction (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.).

7. As per claim 8:

Park disclosed the method of claim 7 wherein providing the first processor with a supported instruction comprises loading the supported instruction in decode logic of the first processor (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The instruction is loaded into the decoder of the coprocessor through the coprocessor instruction register.).

8. As per claim 9:

Park disclosed the method of claim 7 further comprising detecting patterns of supported and unsupported instructions yet to be executed to determine when to perform said providing the first processor with a supported instruction that is executable

in the first processor without the first processor fetching said instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects a supported instruction of the coprocessor and sends it to the coprocessor without it fetching the instruction.).

9. As per claim 10:

Park disclosed the method of claim 9 wherein said patterns comprise an unsupported instruction followed by less then a threshold number of consecutive supported instruction before the next unsupported instruction (Park: Figure 1 element 113, column 4 lines 1-30).

10. As per claim 11:

Park disclosed a system, comprising:

A first processor having fetch logic and decode logic, the first processor fetches supported instructions from memory using said fetch logic and decodes said supported instructions with said decode logic (Park: Figure 1 element 120, column 3 lines 26-37)(The coprocessor is the first processor and has fetch and decode abilities.);

A second processor, the second processor executes unsupported instructions (Park: Figure 1 element 110, column 3 lines 26-37);

Means for loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.);

Means for coordinating when said loading a supported instruction in said decode

logic of the first processor so that the first processor decodes but does not fetch the supported instruction occurs (Park: Figure 1 elements 110 and 113, column 4 lines 31-48)(The CPU detects a coprocessor instruction by the predecoder, and sends it to the coprocessor without the coprocessor fetching the instruction. Thus having the same functionality.).

11. As per claim 12:

Park disclosed the system of claim 11 wherein said means for loading a supported instruction in said decode logic of the first processor so than the first processor decodes but does not fetch the supported instruction comprises coupling the decode logic to a port addressable by the second processor, wherein the second processor fetches the supported instruction and loads said supported instruction in the decode logic of the first processor by accessing said port (Park: Figure 1 element 121, column 4 lines 31-48)(A port is an interface which data is transferred from one computer to another. The register file allows data to be transferred from one processor to another. Thus having the same functionality.).

12. As per claim 14:

Park disclosed the system of claim 11 wherein said means for coordinating when said loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction occurs comprises a control program that examines patterns of supported and unsupported instructions yet to be executed and causes the first processor to switch between multiple instruction execution modes according to the patterns (Park: Figure 1 element

113, column 4 lines 1-30)(The predecoder detects a supported instruction of the coprocessor and sends it to the coprocessor without it fetching the instruction.), wherein said loading a supported instruction in the decode logic of the first processor so that the first processor decodes but does not fetch the supported instruction is one of said multiple instruction execution modes (Park: Figure 1 element 121, column 4 lines 31-48)(The CPU sending instructions to the coprocessor is one mode of execution.)

13. As per claim 15:

Park disclosed the system of claim 14 wherein said control program runs on the second processor (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder is located on the CPU.).

14. As per claim 16:

Claim 16 essentially recites the same limitations of claim 10. Therefore, claim 16 is rejected for the same reasons as claim 10.

New Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

16. Claims 18-23 and 25-27 are rejected under 35 U.S.C. §102(e) as being anticipated by Park et al. (U.S. 6,832,305).

17. As per claim 18:

Claim 18 essentially recites the same limitations of claim 7. Claim 18 additionally recites the following limitations:

Detecting patterns of supported and unsupported instructions yet to be executed (Park: Figure 1 element 113, column 4 lines 1-30)(The predecoder detects a pattern of the next instruction to be executed being a coprocessor or processor instruction.).

18. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 8. Therefore, claim 19 is rejected for the same reason(s) as claim 8.

19. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 9. Therefore, claim 20 is rejected for the same reason(s) as claim 9.

20. As per claim 21:

The additional limitation(s) of claim 21 basically recite the additional limitation(s) of claim 10. Therefore, claim 21 is rejected for the same reason(s) as claim 10.

21. As per claim 22:

Claim 22 essentially recites the same limitations of claim 11. Claim 22 additionally recites the following limitations:

Means for coordinating when said loading a supported instruction in said decode logic of the first processor so that the first processor decodes but does not fetch the

supported instruction occurs comprises a control program that examines patterns of supported and unsupported instructions yet to be executed and causes the first processor to switch between multiple instruction execution modes according to the patterns (Park: Figure 4 element 113, column 4 lines 1-30)(The predecoder detects a pattern of the next instruction to be executed being a coprocessor or processor instruction. The coprocessor switches execution modes when a coprocessor instruction is detected on the processor. It switches from a mode of fetching, decoding, and executing coprocessor instructions in their entirety to a mode of receiving parts of coprocessor instructions from the processor to decode and execute.).

22. As per claim 23:

The additional limitation(s) of claim 23 basically recite the additional limitation(s) of claim 12. Therefore, claim 23 is rejected for the same reason(s) as claim 12.

23. As per claim 25:

The additional limitation(s) of claim 25 basically recite the additional limitation(s) of claim 14. Therefore, claim 25 is rejected for the same reason(s) as claim 14.

24. As per claim 26:

The additional limitation(s) of claim 26 basically recite the additional limitation(s) of claim 15. Therefore, claim 26 is rejected for the same reason(s) as claim 15.

25. As per claim 27:

The additional limitation(s) of claim 27 basically recite the additional limitation(s) of claim 16. Therefore, claim 27 is rejected for the same reason(s) as claim 16.

Maintained Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305).

28. As per claim 17:

Park disclosed the system of claim 16.

Park failed to teach wherein said threshold number is three.

However, it would have been obvious to one of ordinary skill in the art that the threshold number could be 3. By making the threshold 3, the coprocessor could disable fetching because it knows that instructions will be received from the CPU. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a threshold of 3 to avoid wasteful processing.

29. Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of Chaudhry et al. (U.S. 6,681,318).

30. As per claim 13:

Park disclosed the system of claim 12.

Park failed to teach wherein a switch permits said coupling the decode logic to the port addressable by the second processor.

However, Chaudhry disclosed wherein a switch permits said coupling the decode logic to the port addressable by the second processor (Chaudhry: Figure 1 element 110, column 4 lines 37-41)(The switch is coupled to two processors and indirectly coupled to the decode unit in each of the processors.).

An advantage of using a switch is that it can be turned off when it's not being used. This would be advantageous to Park's system of connecting data between the processors so that the bus line connecting the processors to transferring instructions could be turned off when it's not being used. One of ordinary skill in the art would have been motivated to use a switch between the processors to control data flow so that data isn't needlessly transferred between the processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a switch between the CPU and coprocessor of Park for the advantage of turning off the data flow between the two when it's not needed.

New Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claim 28 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305).

33. As per claim 28:

The additional limitation(s) of claim 28 basically recite the additional limitation(s) of claim 17. Therefore, claim 28 is rejected for the same reason(s) as claim 17.

34. Claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of Chaudhry et al. (U.S. 6,681,318).

35. As per claim 24:

The additional limitation(s) of claim 24 basically recite the additional limitation(s) of claim 13. Therefore, claim 24 is rejected for the same reason(s) as claim 13.

Response to Arguments

36. The arguments presented by Applicant in the response, received on 9/26/2006 are not considered persuasive.

37. Applicant argues "Park failed to teach providing the first processor with a supported instruction that is executable in the first processor without the first processor fetching said instruction" for claims 7 and 11.

This argument is not found to be persuasive for the following reason. Applicant also pointed out that Park has part of the coprocessor instruction being fetched into the coprocessor fetch buffer, with the other half coming from the processor. The examiner agrees that this is the case, but disagrees that this doesn't read upon the claimed limitation. The claimed limitation recites the first processor not fetching the instruction, being the entire instruction and not half or part of the instruction. Since the coprocessor doesn't fetch the entire coprocessor instruction, Park still reads upon the claimed

limitation. Additionally for claim 11, figure 4 shows the processor fetched part of the coprocessor instruction being sent to the decoder of the coprocessor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100